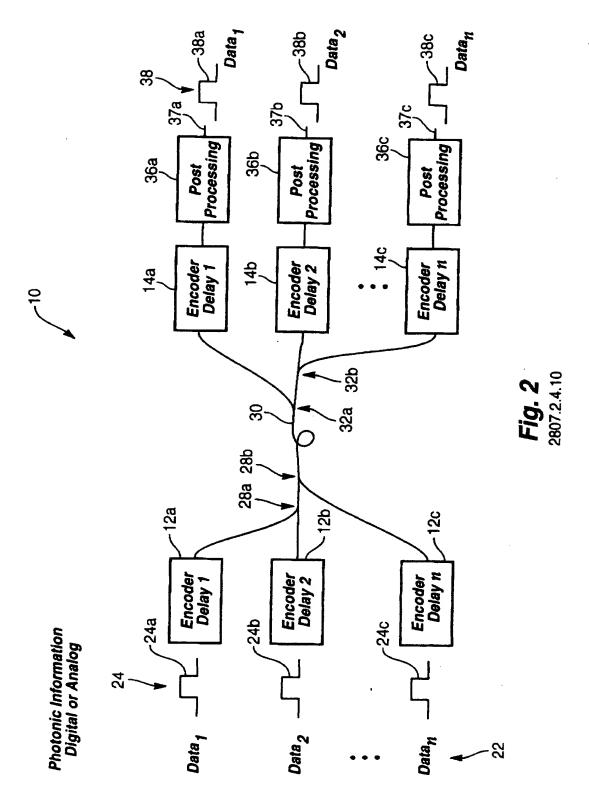
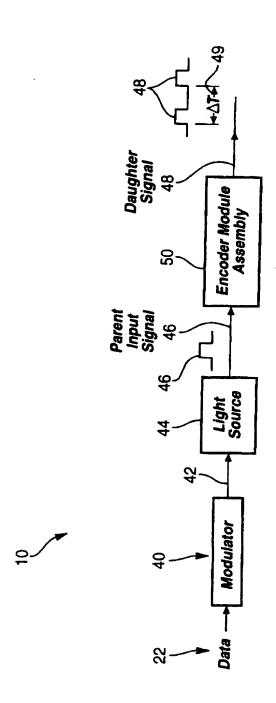


**FIG. 1** 2807.2.4.10



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j



Differential Delay Multiplexer Sender/Encoder

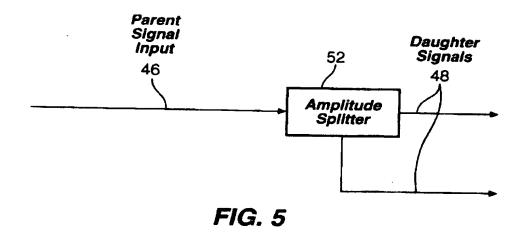
**Fig. 3** 2807.2.4.10

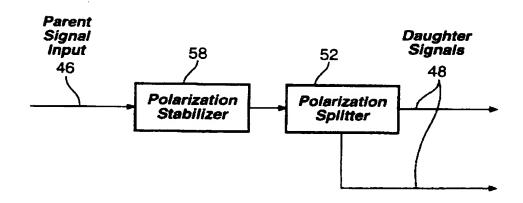
Differential Delay Multiplexer (DDM) Sender/Encoder

55b

Fig. 4 2807.2.4.

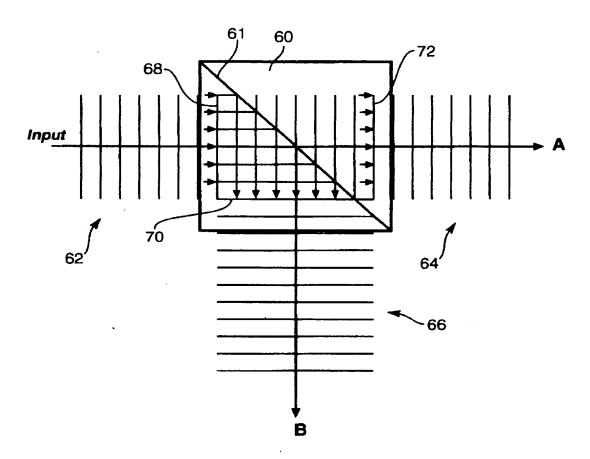
2:





**Splitting Criteria** 

FIG. 6 2807.2.4.



**Amplitude or Polarization Splitter** 

FIG. 7 2807.2.4.

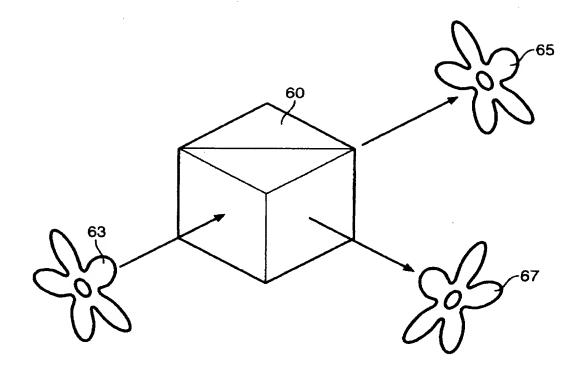
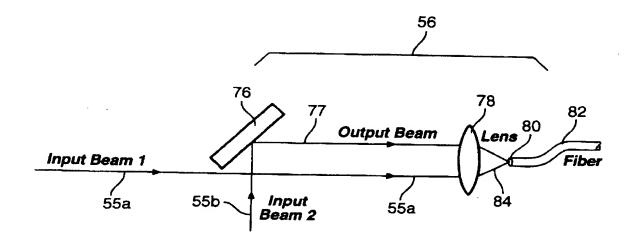


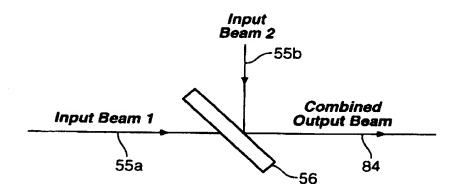
Image Signals Which Maintain Spatial Information

FIG. 7A

2807.2.4.

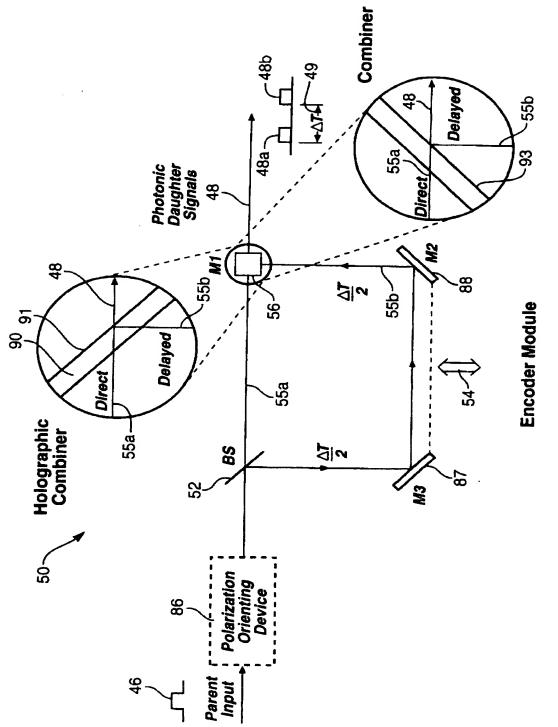


Beam Combiner FIG. 8

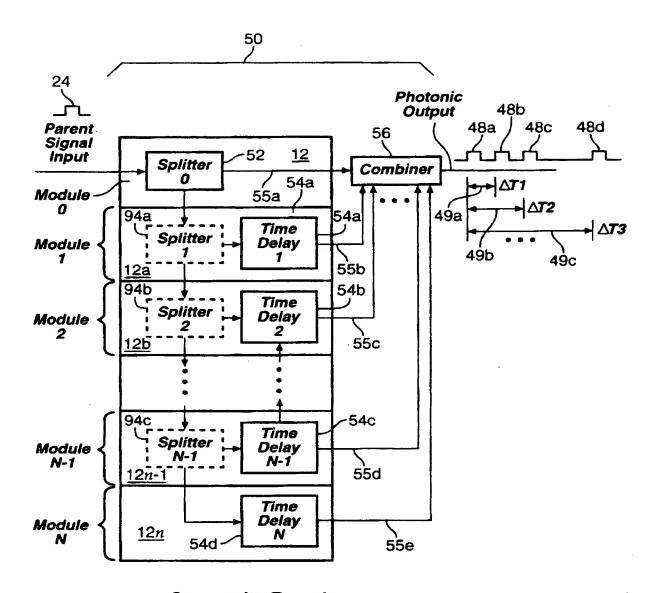


**Amplitude or Polarization Combiner** 

FIG. 9 2807.2.4.



**Fig. 10** 2807.2.4.



Composite Encoder Module Assembly

FIG. 11 2807.2.4.

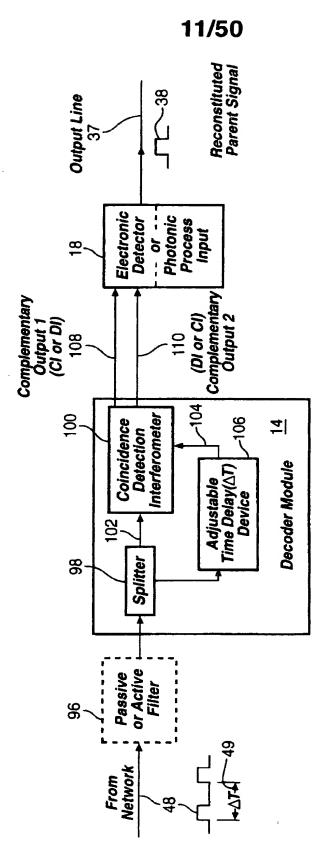


Fig. 12

----

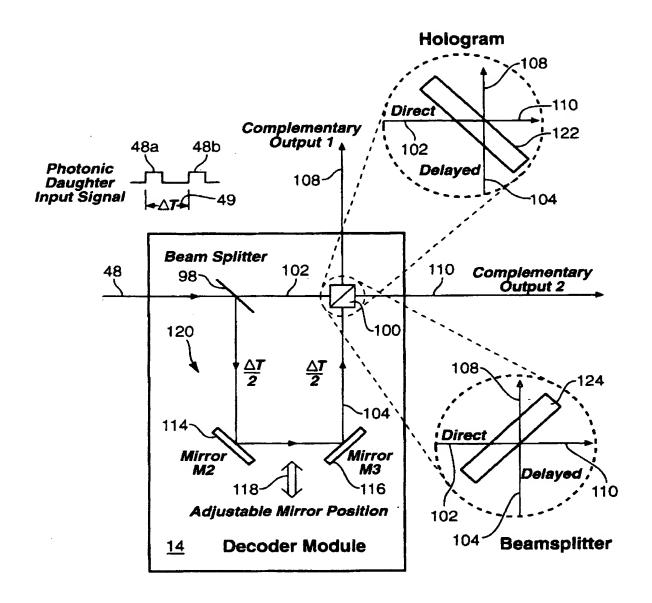


FIG. 13

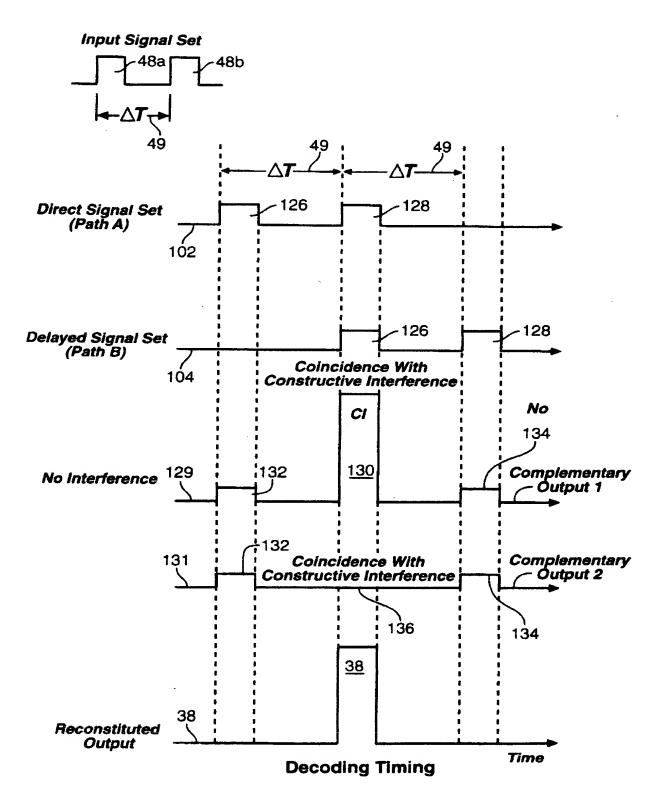


FIG. 14

48

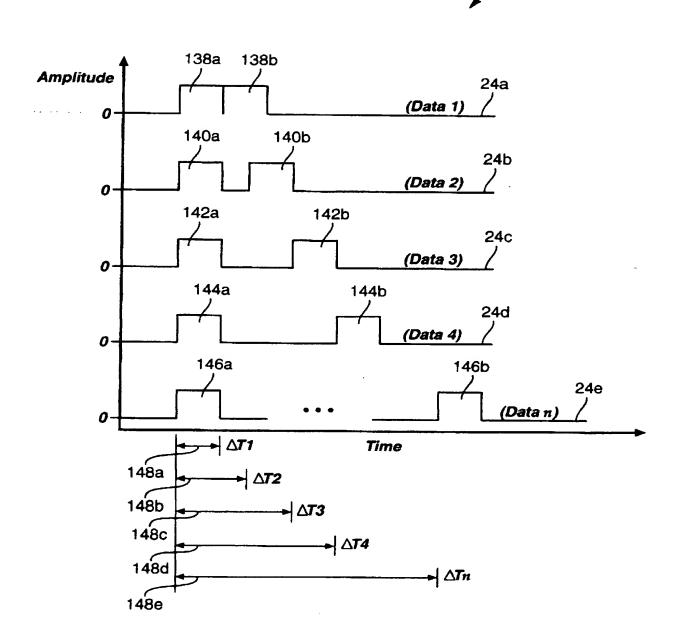


Fig. 15

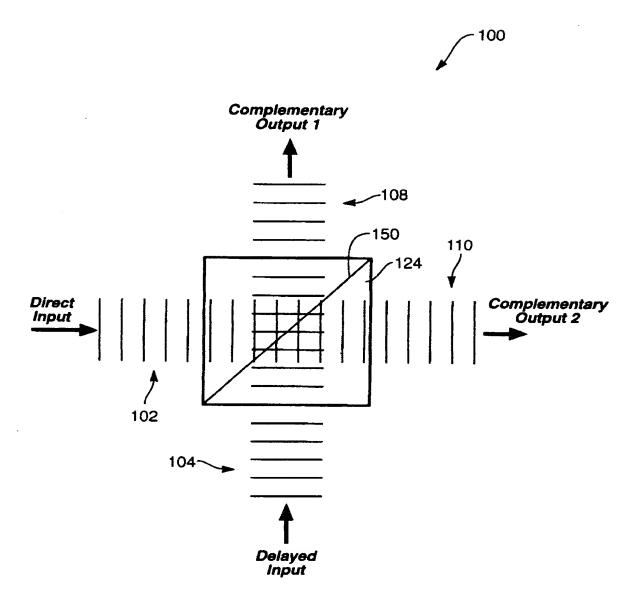


Fig. 16

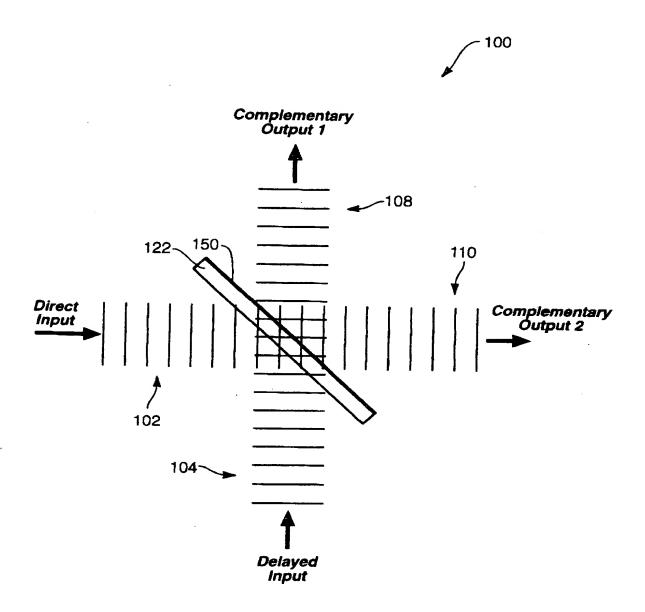


Fig. 17

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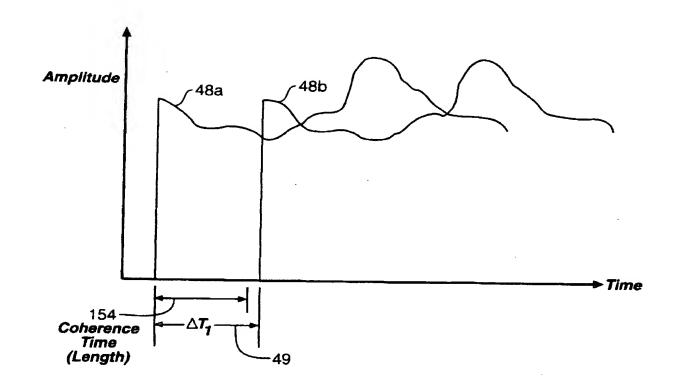


Fig. 18

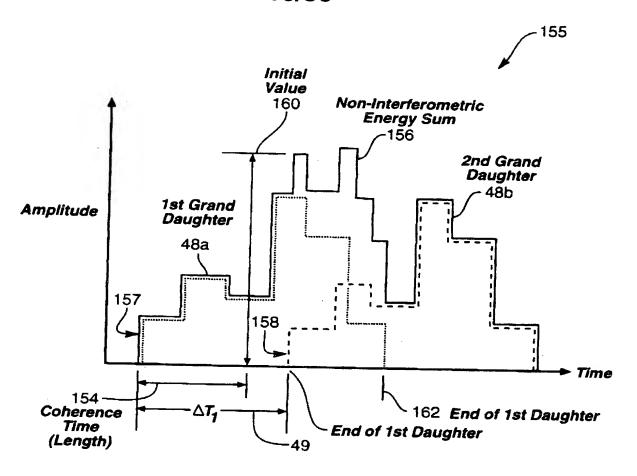


Fig. 19

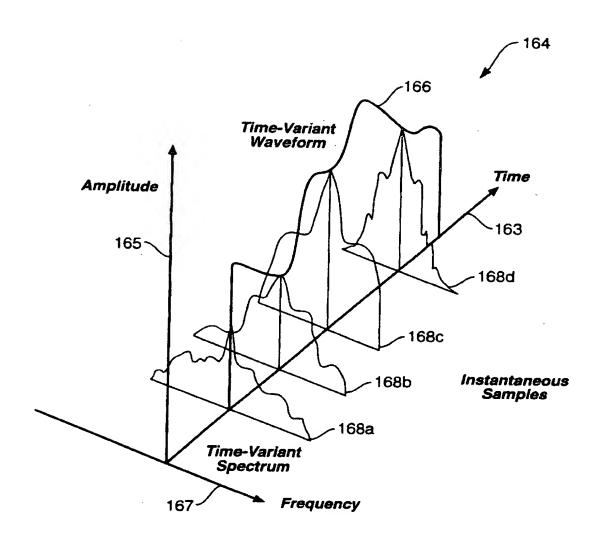


Fig. 20

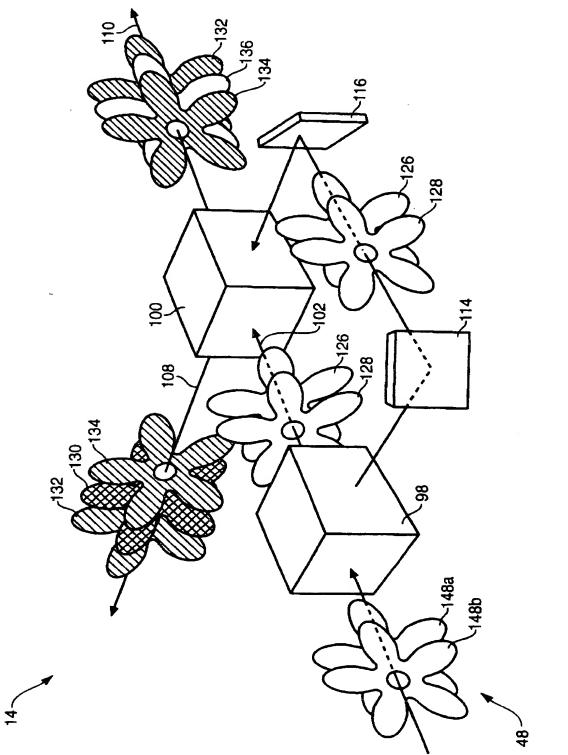
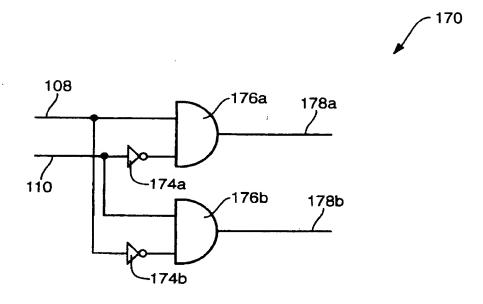


Fig. 21



Photonic Processor Fig. 22

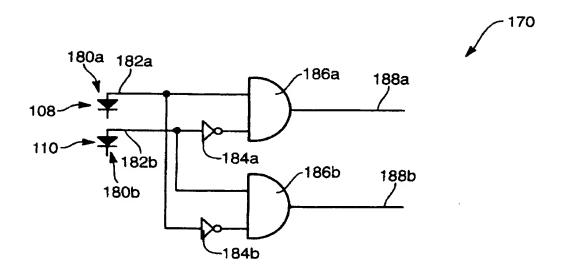


Fig. 23A



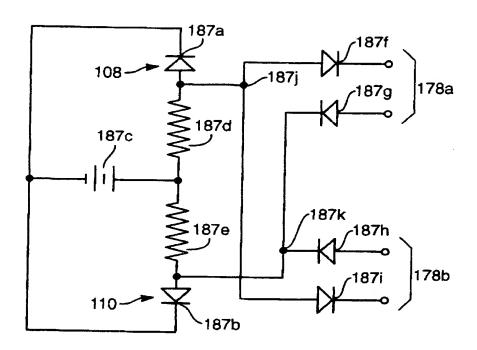
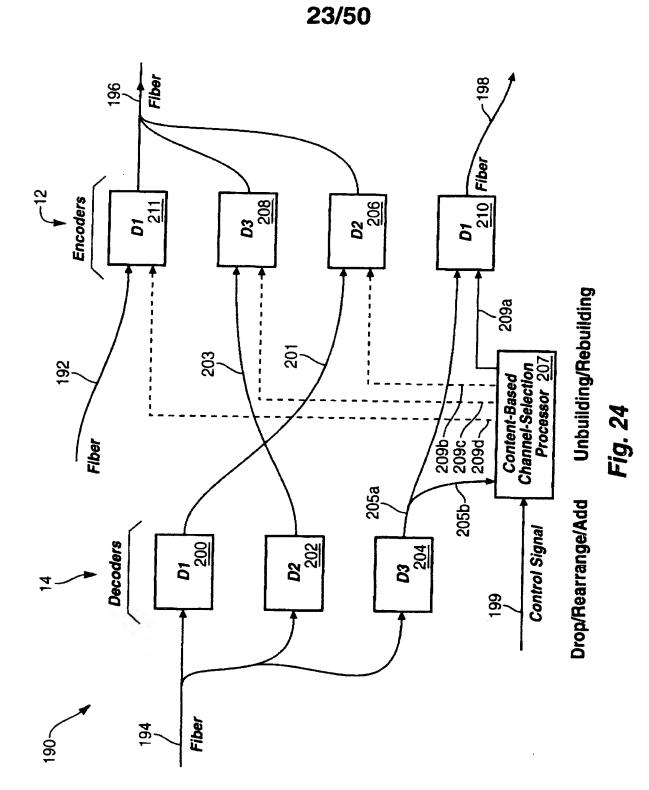
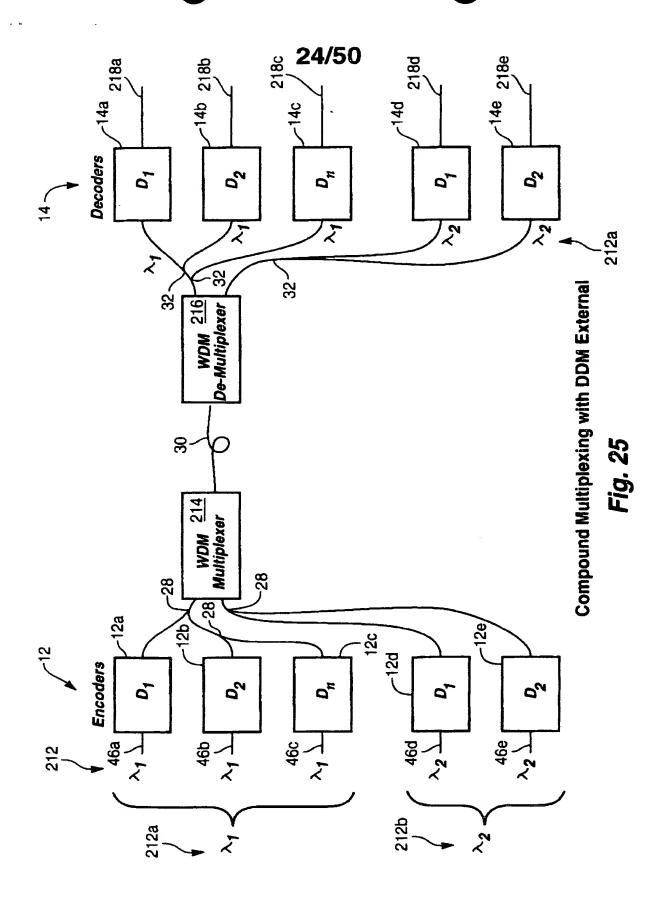
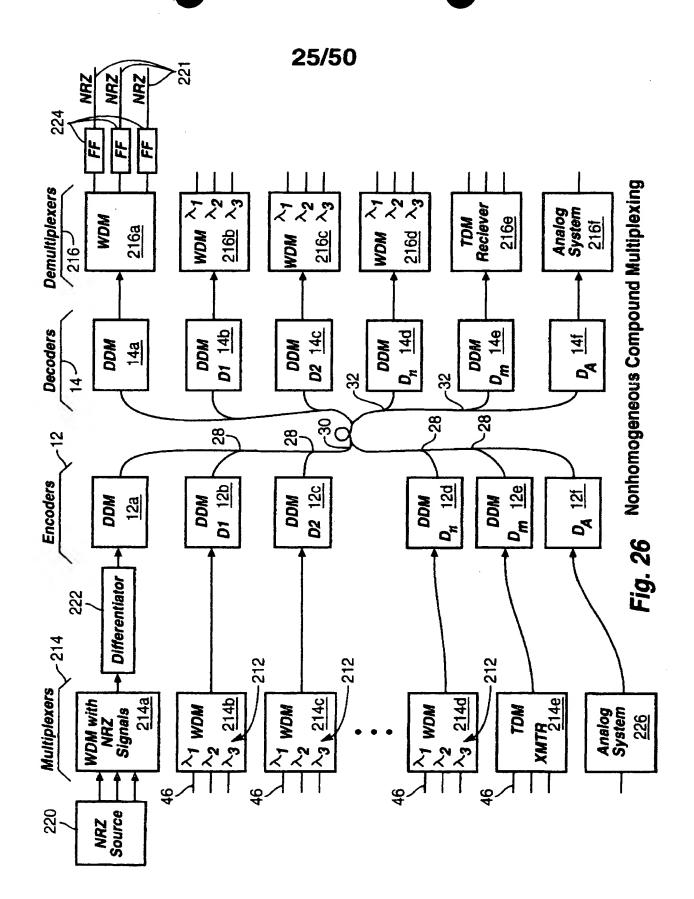
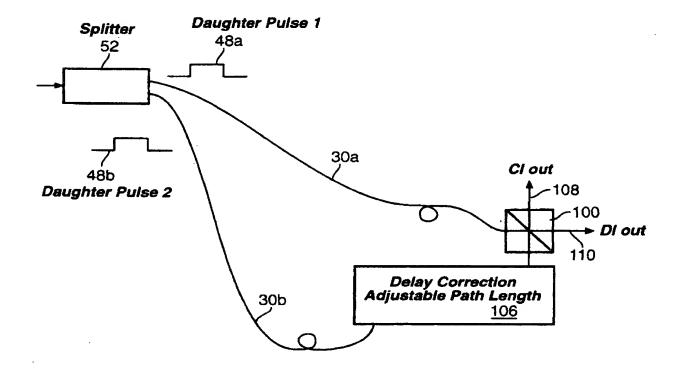


Fig. 23B







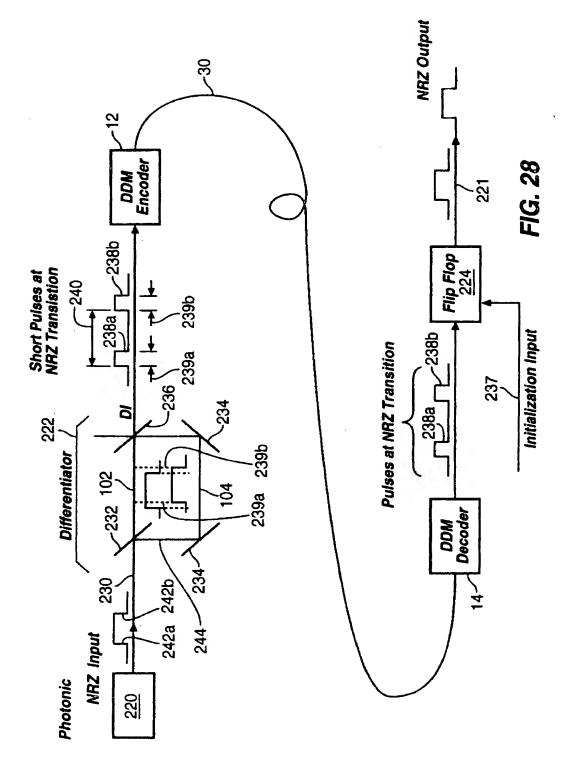


**Multiple Delay Path** 

Integrated Delay and Delay Correction

FIG. 27

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Photonic NRZ Interface

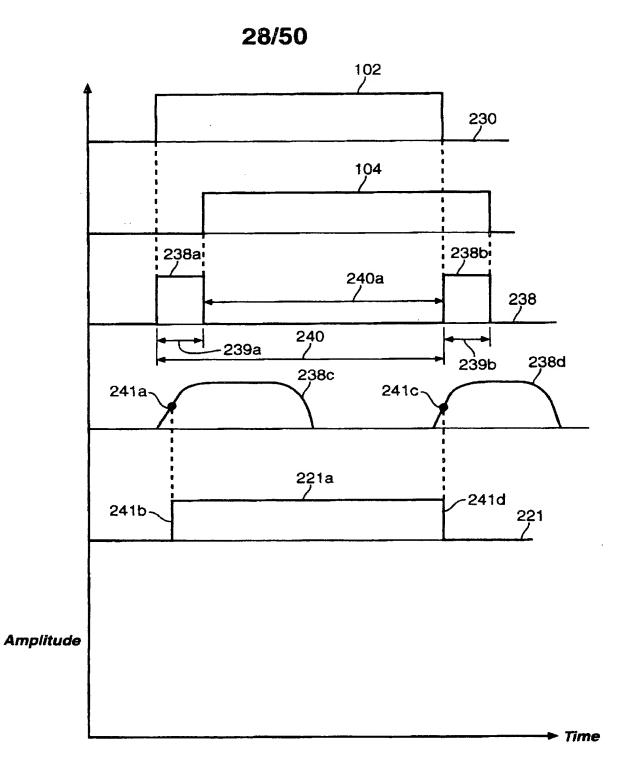
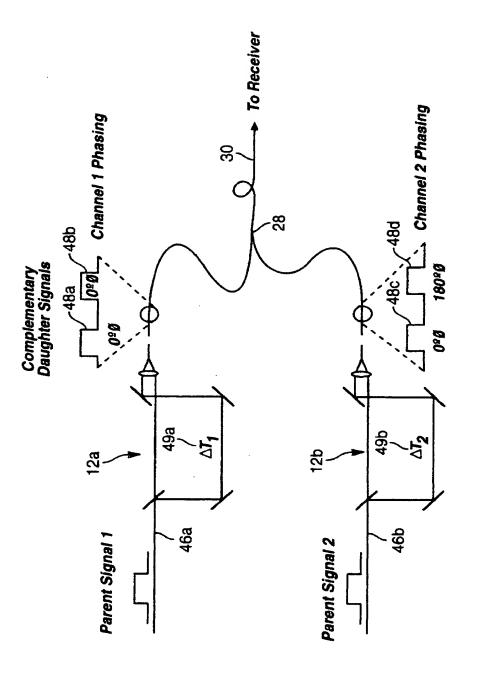


FIG. 29



Phase Sequenced Dual Channel Encoder

FIG. 30

Phase Sequenced Dual Channel Decoder

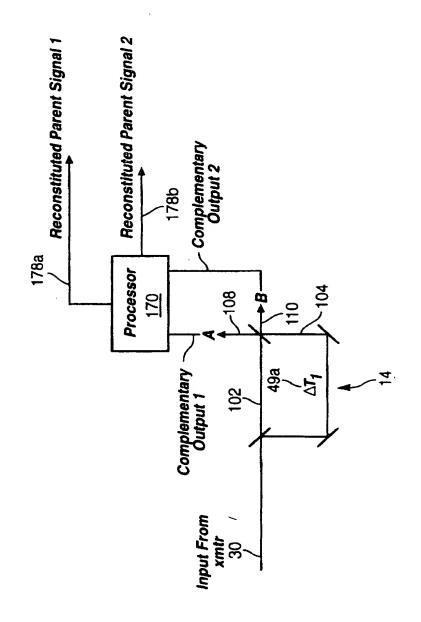


FIG. 31

#### **Phase Sequence Timing**

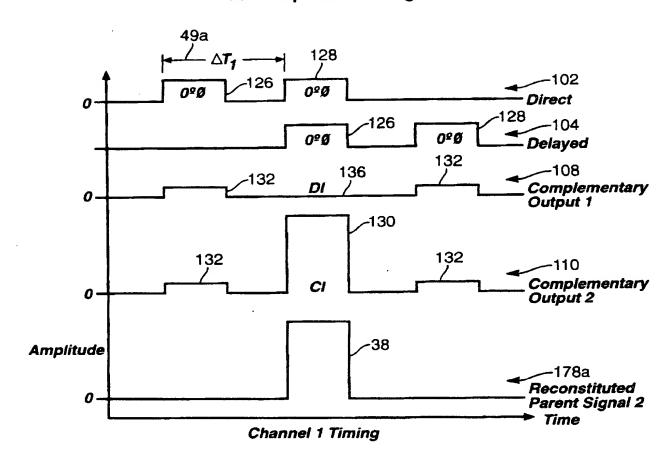


FIG. 32

### **Phase Sequence Timing**

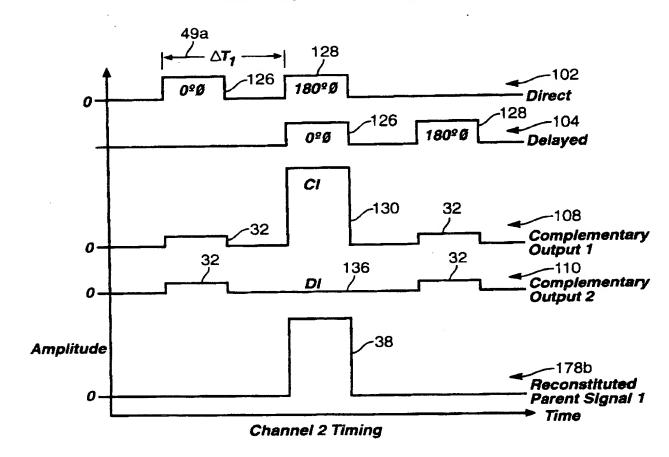
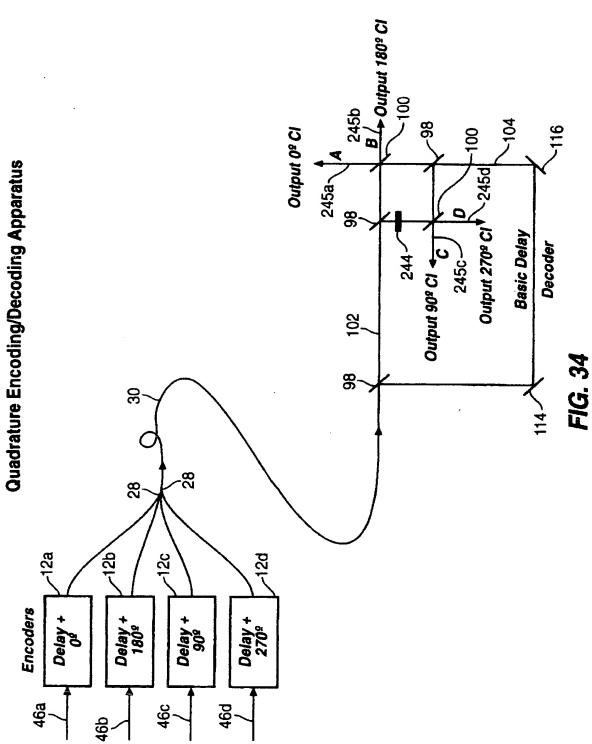


FIG. 33

OOZEL ECHELZOO



	Phase of Direct Signal	Phase of Delayed Signal	Quadrature Outputs			
46a			A	В	С	D
Channel 1	0	0	CI	DI	<b>C</b> =	: D
Channel 2	0	180	Di	CI	<b>C</b> =	. D
Channel 3	0	90	A =	B	CI	DI
Channel 4	0	270	A =	В	DI	CI
			245a	245	245	c 245d

FIG. 35

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Quadrature Wave Forms For One Channel

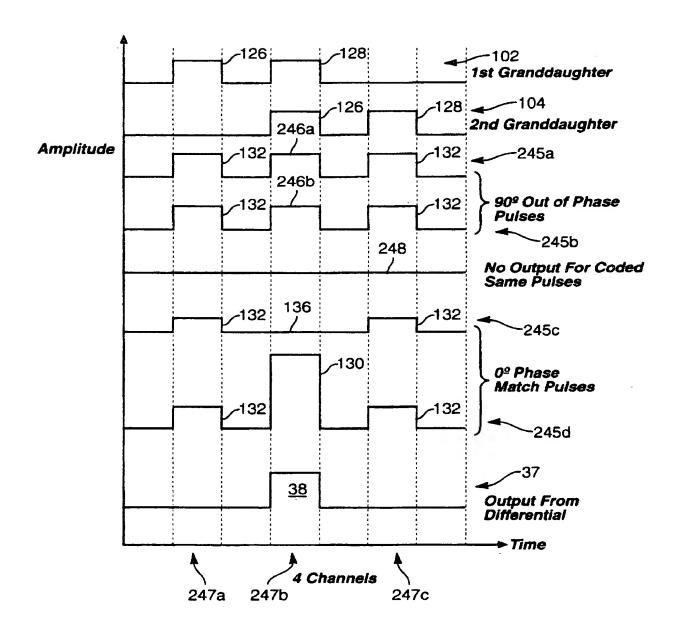


FIG. 36

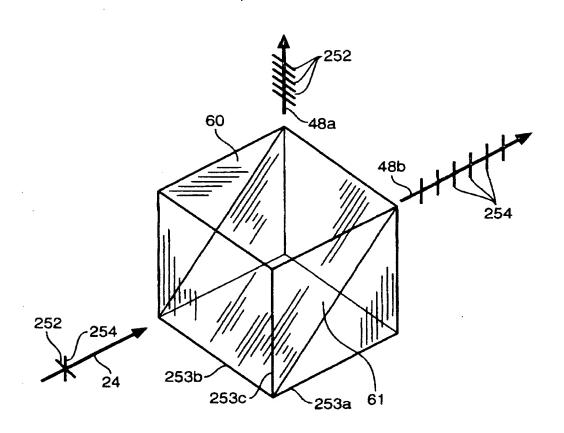


FIG. 37A

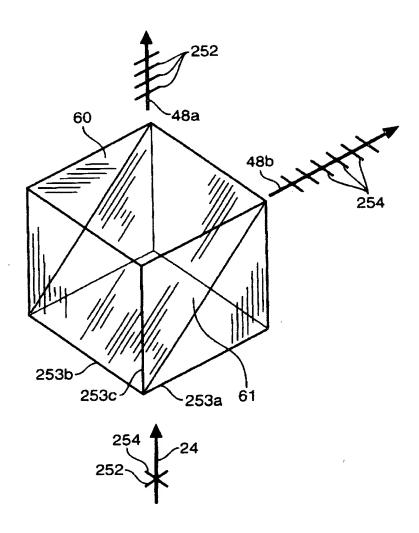
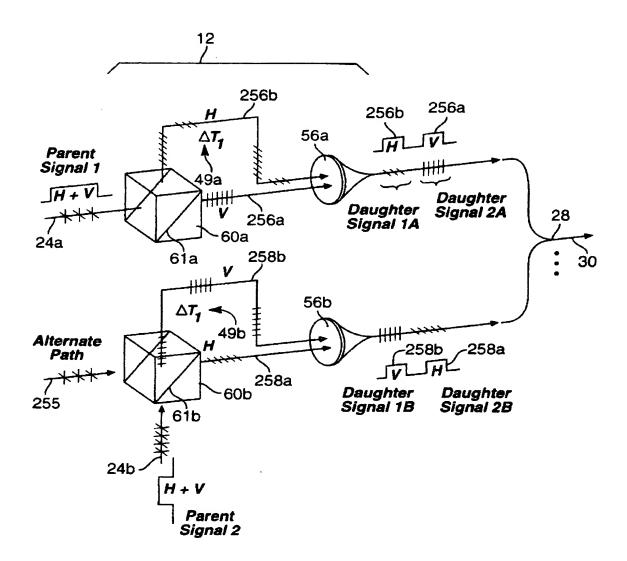
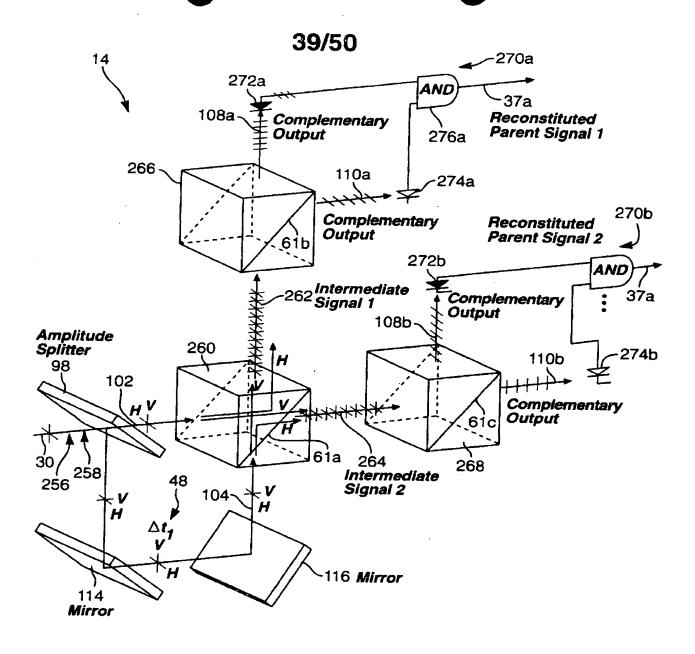


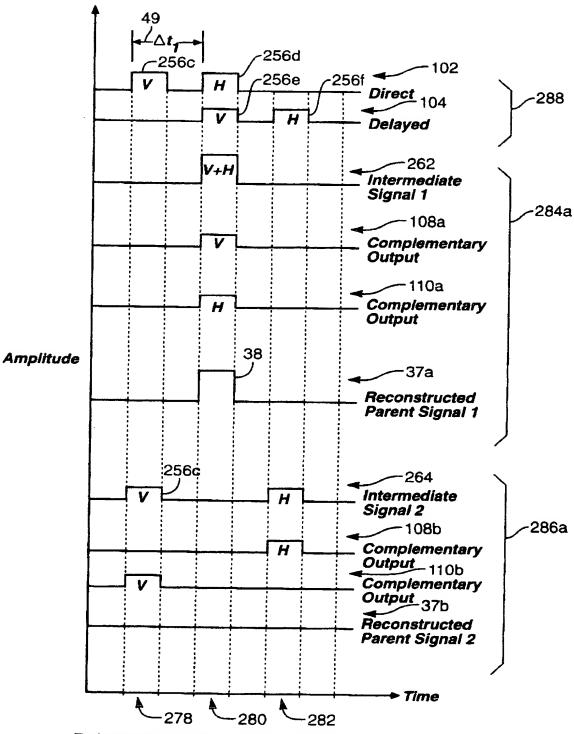
FIG. 37B



Double Encoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Double Decoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Polarization Sequenced Channel 1 Timing FIG. 40

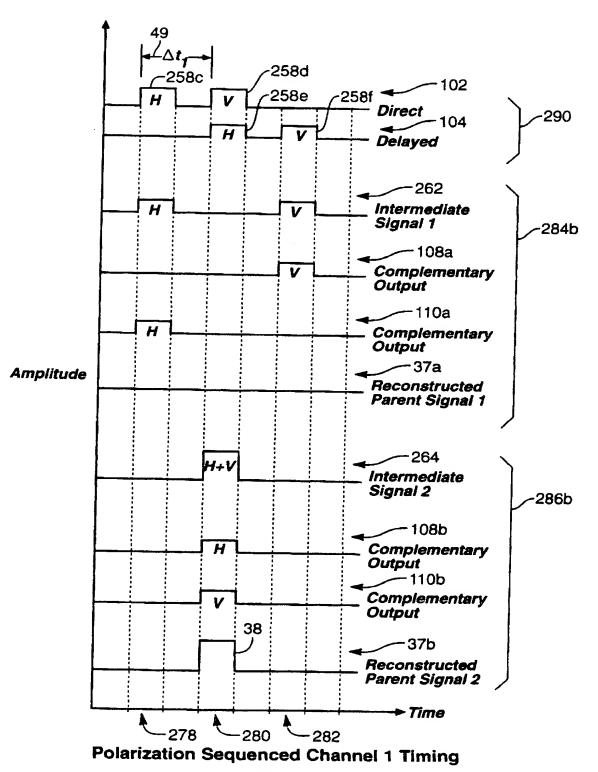


FIG. 41

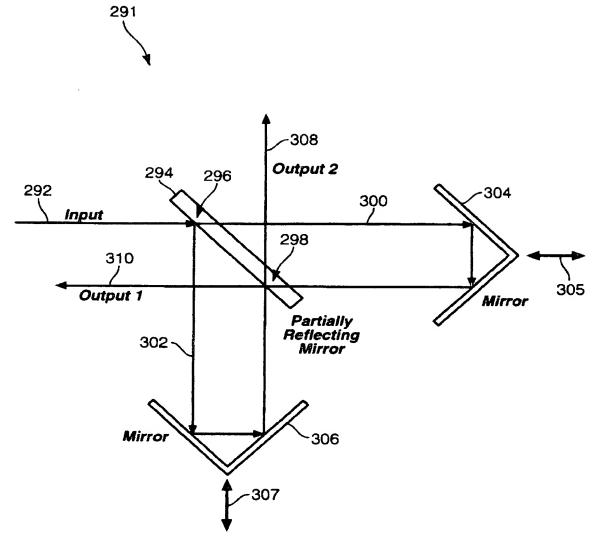
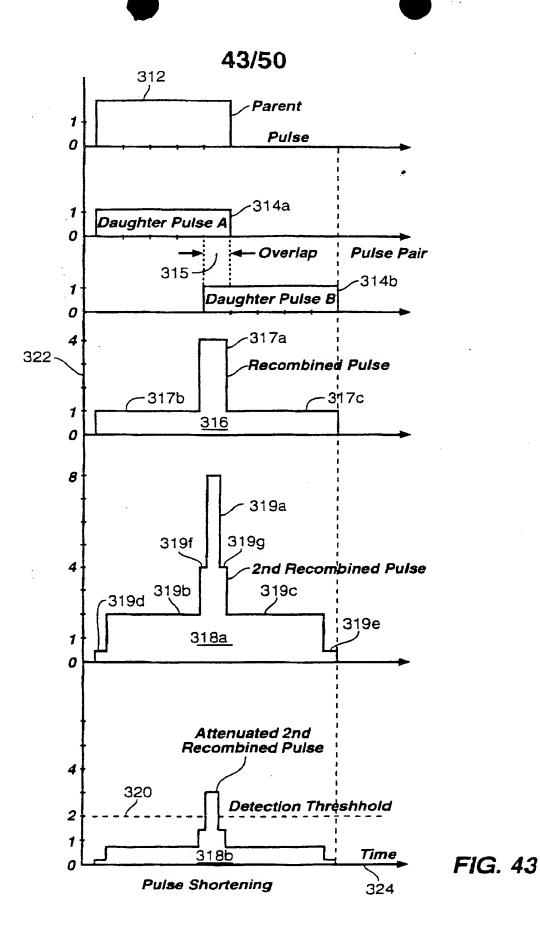


FIG. 42



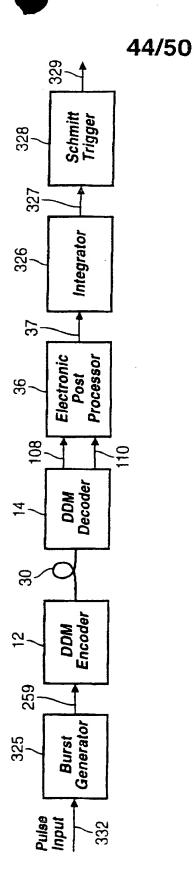


FIG. 44

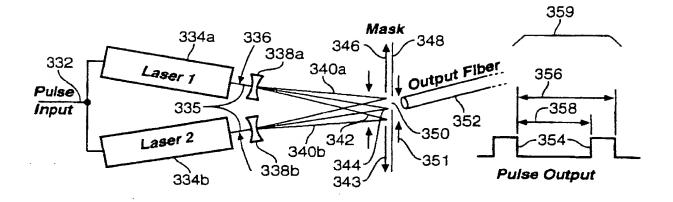


FIG. 45

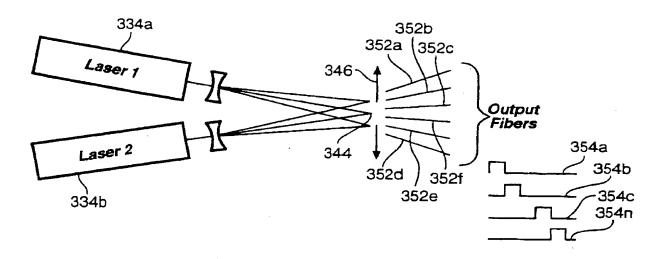


FIG. 46

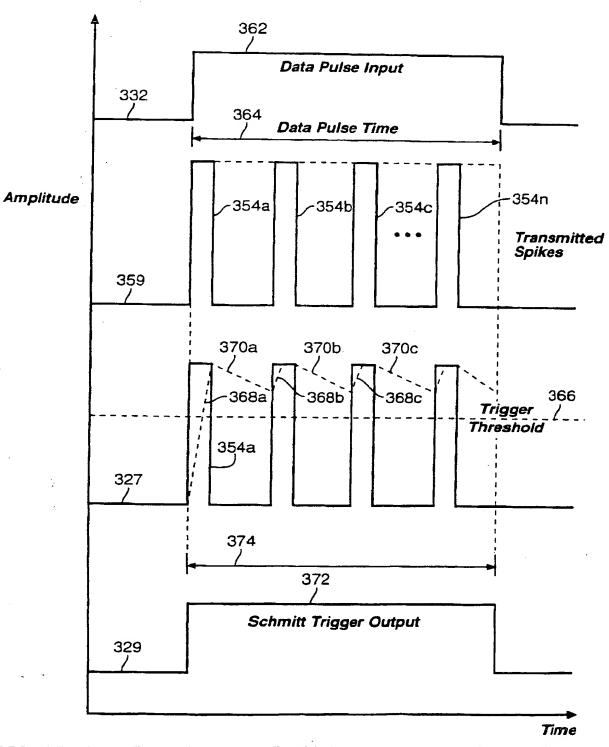
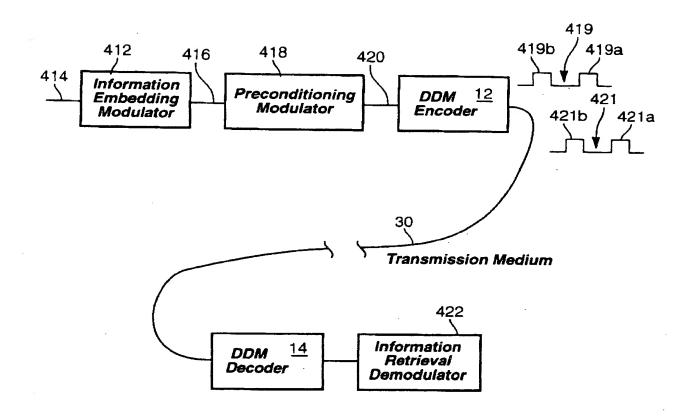


FIG. 47





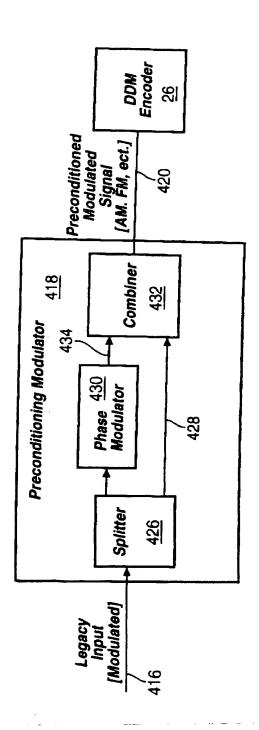


FIG. 49

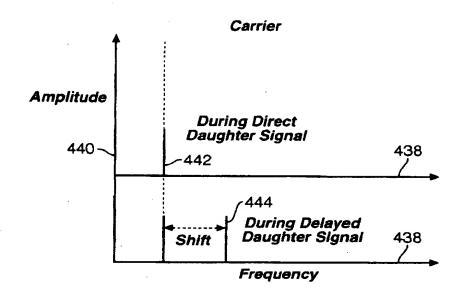


FIG. 50